AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1. (previously presented): A base station of a radio-operated telecommunications system comprising:

a receiver processing received information; and

one or more digital signal processors, wherein each of said digital signal processors is configured to perform a symbol rate processing and at least parts of a chip rate processing.

2. (previously presented): The base station as claimed in Claim 1, wherein the signal processor is also configured to perform a task allocation for controlling the chip rate processing and the symbol rate processing.

3. (original): The base station as claimed in Claim 1, the signal processor being designed such that firstly the chip rate processing and then the symbol rate processing can be performed.

4. (original): The base station as claimed in Claim 1, wherein an array or group of digital signal processors is provided.

5. (original): The base station as claimed in Claim 4, wherein the chip rate processing and the symbol rate processing can be distributed between sub-arrays or sub-groups of signal processors.

6. (original): The base station as claimed in Claim 1, wherein at least one memory is provided which is suitable for and provided for the intermediate storage of the received information.

7. (previously presented): The base station as claimed in Claim 1, wherein the chip rate processing comprises a despreading of the received information and wherein the signal processor is configured to dispread the received information.

8. (previously presented): The base station as claimed in Claim 1, wherein the symbol rate processing comprises a decoding of the received information.

9. (previously presented): A receiver for a base station of a radio-operated telecommunications system for processing received information with one or more digital signal processors, wherein each of said digital signal processors is configured for performing a symbol rate processing and at least parts of a chip rate processing.

10. (previously presented): A digital signal processor configured to execute symbol rate processing for a receiver of a base station of a radio-operated telecommunications system, wherein the signal processor is configured to perform at least parts of a chip rate processing.

11. (previously presented): A radio-operated telecommunications system comprising at least one of:

a base station having one or more digital signal processors, wherein each of the digital signal processors is configured to perform a symbol rate processing and at least parts of a chip rate processing;

a receiver processing received information having said one or more digital signal processors; and

said one or more digital processors.

12. (previously presented): A process for operating a radio-operated telecommunications system, wherein information received by a base station is subjected to a symbol rate processing by one or more digital signal processors, wherein at least a part of the chip rate processing is performed by same processor from the digital signal processors.

13. (original): The process as claimed in Claim 12, wherein firstly the chip rate processing and then the symbol rate processing is performed.

14. (original): The process as claimed in Claim 12, wherein a task allocation for controlling the chip rate processing and the symbol rate processing is performed by the at least one signal processor.

15. (original): The process as claimed in Claim 12, wherein an array or group of digital signal processors is provided, the chip rate processing and the symbol rate processing is distributed between sub-arrays or sub-groups of signal processors.

16. (original): The process as claimed in Claim 15, wherein the distribution of the array or group of signal processors between the chip rate processing and the symbol rate processing is performed by the task allocation.

17. and 18. (canceled).

19. (previously presented): The telecommunication system according to claim 11, wherein the telecommunication system is a code division multiple access (CDMA) telecommunications system.

20. (currently amended): A digital signal processor comprising:

means for executing symbol rate processing;

means for executing chip rate processing; and

means for switching over from said means for executing symbol rate processing to said means for executing chip rate processing,

wherein the digital signal processor is a single digital processor having the symbol rate processing means, the chip rate processing means and the switching means and wherein the digital signal processor is disposed inside a receiver.

21. (previously presented): The digital signal processor according to claim 20, wherein the means for switching instructs for transmission of information in the digital processor first to the means for executing chip rate processing and then to the means for executing symbol rate processing.

22. (new): The base station according to claim 1, wherein each of said digital signal processors is configured to perform the symbol rate processing comprising decoding the received information and at least said parts of the chip rate processing comprising despreading the received information.

23. (new): The base station according to claim 22, wherein said despreading comprises separating the received information based on sources of the received information and assigning the separated received information to a respective source.

24. (new): The digital signal processor according to claim 20, wherein said symbol rate processing means decode the received information and wherein said chip rate processing means despread the received information.